A Systematic Approach to Qualification of 90 nm Low-K Flip-Chip Packaging

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Abstract

Challenges associated with Low-K flip-chip packaging arise from properties inherent with the dielectric material properties, i.e., lower strength, lower adhesions, and higher TCE (as compared to FSG dielectrics). In order to assemble and qualify a reliable and robust package, a lot of attention needs to be focused on items like material selection, bump type and bump distribution. This paper explains the step by step approach taken by Avago Technologies Imaging Systems Division (ISD), in partnership with Amkor Technology to successfully qualify a production ready process for 90 nm Low-K flip chip using both ceramic HITCE and built-up laminate substrate technologies. This was implemented successfully on a new set of advanced laminate material with stacked vias and via on plated thru hole and eliminated Electroless Nickel Immersion Gold (ENIG) surface finish. Details of the test vehicles used and the test programs have been provided as well. The experiments will be discussed in detail, along with the assembly process steps and the underfills used, focusing on the properties that are important to stress reduction. The reliability test results – JEDEC for the component level tests (pop corning, temperature cycle, high temperature storage and biased HAST) are also presented. The process robustness was addressed by extending the reliability test read points to 2000 temperature cycles and 2000 hours of high temperature storage. Failure analysis results will be discussed where appropriate. Finally, the qualification results with the frozen process are presented and discussed.

Introduction

The obvious reasons for going into Copper interconnect and Low-K in integrated circuits is to obtain better electrical performance (speed, crosstalk, power). Avago Technologies Imaging Systems Division (ISD) in Fort Collins, Colorado has had considerable experience in developing and qualifying high performance flip-chip packages on a variety of wafer fabrication technology nodes (0.25 microns, 0.18 microns and 0.13 microns – all FSG), successfully qualifying these packaging technologies and shipping in volume, products that encompass networking, computing and storage. ISD's business model relies on working with external wafer Fabs and assembly sub-contractors for developing and qualifying packaging technologies to enable our business.

All prior silicon technologies were FSG, so not much could be leveraged, since Low-K is unlike anything else that ISD has ever worked with before, (lower strength, lower adhesion and higher TCE as reported by others[1,2], than the previous generation of dielectrics) which could potentially result in delamination[3,4] within the die (and hence a failure) induced by package related stresses (underfill, substrate material, bump type, lid etc). The other critical items that needed to be investigated included wafer saw, chip attach reflow profile, underfill reflow and curing, lid (heat spreader) attach and ball attach (assembly process flow steps).

The markets addressed by ISD are the high end ASICs; the die and package are both large and complex. Typical die sizes range from 14 mm to 18 mm on a side and the package sizes range from 25 mm to 52 mm. The substrate technologies for these markets are Alumina ceramic, High Thermal Coefficient of Expansion (HITCE) ceramic and Surface Laminar Circuit (SLC) laminate, which are required for product electrical and thermal performance. Also investigated were various design in the SLC substrate (via on plated thru hole, stacked via on plated thru hole, stacked via in the buildup) as one of the variables – to further improve the electrical performance and routability for this substrate technology.

Based on prior reliability testing and qualification experience, JEDEC standards were followed for environmental testing, i.e., temperature cycle, high temperature storage and moisture resistance, starting at the very beginning of this evaluation (screening experiments followed by assembly optimization), to avoid any surprises during the final qualification testing.

This paper describes in detail, the structure of the test vehicles used, the properties of the underfills, bump type and structure, important assembly parameters, test results, failure analysis results where applicable, the systematic approach on the design of experiments for the screening experiments and assembly optimization, and the finalized set of materials used to successfully complete JEDEC level qualification and getting the process production ready

Materials and Methods

For this undertaking, Avago Technologies worked in partnership with Amkor Technology to identify the appropriate test vehicles, assembly parameters, materials selection, bump configuration and Design of Experiments (DOE's). The following approach was used to start this work:

- Bump geometry optimization experiment (non-underfill parts)
- Screening experiments (assembly parameters and underfills) or 1st Cycle of Learning (COL)
- Assembly optimization or 2nd COL
- Verification builds (if required)
- JEDEC level qualification for package

Some key elements to this study were – bump layout, bump structure and underfill. Knowing the nature of the Low-

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K silicon and the materials that they were interfacing with (primarily the Alumina Ceramic and HITCE Ceramic), these two items are critical, especially selecting the appropriate underfill material. Modeling studies and studies published by others[5,6] show that the optimum underfill should have a reduced glass transition Tg (~ 70 ^{o}C) and a Young modulus of ~ 8 GPa. It was also important (from a manufacturing perspective) that the underfill flows well so as not to impact thru-put at the underfill operation.

Test Vehicles

Based on the inputs received from our internal Design Center and from manufacturing, the following test chip evolved.

Silicon

Standard TSMC 90 nm with a final passivation of silicon nitride over silicon oxide, four levels of metal with two Low-K and two un-doped silicon inner layer dielectric, copper with Al cap, 200 micron C4 pad pitch in the periphery and 400 microns internal – full array (to alleviate stresses associated with uneven bump distribution). Package Sizes:

17 mm x 17 mm for ceramic (HITCE and Alumina)
17 mm x 15 mm for laminate (SLC)

The two die were juxtaposed to create a multi die reticle so as not to create two mask sets. The extra space available on the reticle was used to populate die for electromigration studies. Both these die included daisy chains, Kelvin structures, die crack detector and delamination structures (see Figure 1).

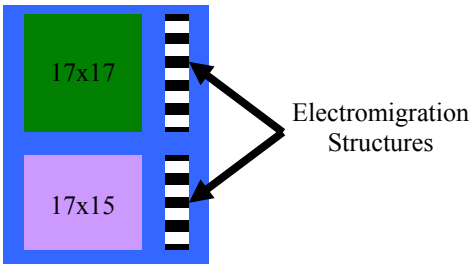

Figure 1. Layout of test die.

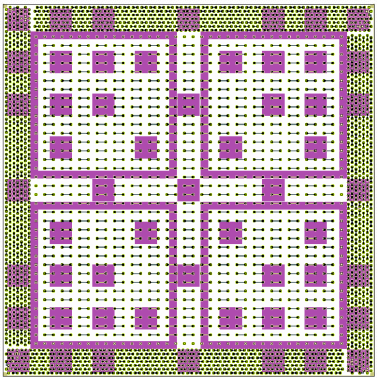

Figure 2. Bump layout on die.

The test chip was a metal-only test chip with no active structures, and consisted of seven rows of daisy chain, Kelvin structures, temperature sensors, die crack detector, delamination crack detectors and center daisy chains. The under bump metallurgy was the same; however, the copper pad size, passivation opening and Aluminum cap varied across the die. The same pattern was used for both the SLC and HITCE die (See Figure 2).

Daisy Chains

Daisy chains are implemented in the top metal layer only. There are seven rows of daisy chains (200 micron pitch) on each of the four sides. There are also four daisy chains (400 micron pitch) in the center of the die.

The chains are formed by alternating links on the die and the substrate and are connected together in rings.

Kelvin Structures

Kelvin (4-point) structures are located in the corner of the die, in the center of the die and on the center edge of the die. These structures permit precise measurement of the resistance of the bumps.

Each Kelvin bump has two package side connections and two die side connections to facilitate the 4-point measurement except for the first and last bump.

Temperature Sensors

The temperature sensors are metal resistors implemented in the top layer and require a 4-point measurement. There are only two temperature sensors, one on the Southeast side and one on the Southwest side. Each terminal in each metal resistor has two packages connections to facilitate the 4-point measurement.

Delamination Crack Detector

Delamination crack detectors are structures that serpentine through the inner layers and are used to detect inner layer low-k delamination. Each corner has six delamination crack detectors; there is also one delamination crack detector in the center of each edge and many delamination crack detectors covering the rest of the die. All the delamination crack detector bumps are located on a ring after the seventh row of daisy chains and are grouped in the four quadrants and the center of the die.

Other Structures on the Package

Die crack detector
Package crack detector
Alignment structures

Bump

The bumping technology used was plated 95/5 PbSn and plated 63/37 SnPb. Prior work was done only using high Pb bumps to address the bump current carrying capacity and the associated electromigration concerns. However, the low-K concerns associated with the 90 nm silicon and stresses associated with high Pb bumps prompted us to consider both these bumps. Under Bump Metallurgy (UBM) consisted of sputtered Titanium, sputtered Copper and plated Nickel. The UBM diameter was 110 microns, with a bump height of 90 microns. The bumping was done at Unitive (Taiwan).

For the 1st COL, the bump mask was created with various passivation openings, top metal pad sizes and aluminum cap sizes (in the four quadrants) for the bump geometry optimization experiment, and the 1st COL as indicated in the previous section. This was done so that the test results could be monitored from each of the quadrants and a determination

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could be made on how they performed in the reliability tests. The optimized bump structure was chosen based on the results from the 1st COL and the Bump Optimization experiment, then the mask was turned to make the bump structures uniform for the 2nd COL and the qualification builds.

Package

SLC – 2-6-2 buildup: two versions were used; the original material set which was qualified in a previous generation (old SLC) and one with the "green" material set (new SLC). The substrate was designed with a 680 micron BGA pad and 500 micron solder mask opening, as well as two different finishes – ENIG (Electroless Nickel, Immersion Gold) and Cu eutectic SOP (Solder On Pad). This was assembled with a two piece lid supplied by Amkor. The SLC substrates were supplied by Kyocera Corporation.

HITCE Ceramic – 14 layers, 2.1 mm thick, 680 micron pad BGA pad. The BGA pad finish was electroless Nickel and electroless Gold. The HITCE substrates were supplied by Kyocera Corporation.

Alumina Ceramic – 14 layer, 2.8 mm thick, 680 micron pad BGA pad. The BGA pad finish was electroless Nickel and electroless Gold. The Alumina ceramic substrates were supplied by NTK.

Package size – 45 mm square, 1.0 mm BGA pitch, for all the three technologies so the same test socket and DUT board are used for electrical test. Figure 3 illustrates the test package layout.

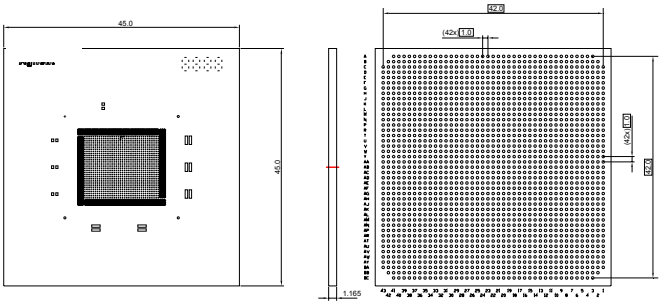

Figure 3. Test package layout.

Electrical Test

The test chip is designed so that all the test structures can be tested using simple resistance. Only the Kelvin structures were measured using a 4-point measurement, the rest of the structures was measured using a two-point measurement.

The test is divided into several sections:

- Alignment test to make sure that the part is seated properly in the socket
- Package crack detector
- Die crack detector
- Periphery Daisy chain
- Center daisy chain
- Leakage
- Kelvin structure
- Delamination crack detector
- Diagnostic test to be run only when one of the seven daisy chains is failing to locate the failing segment of the chain.

The same test software and program was used for the three package platforms since the packages were designed using the same output pin. The electrical test was performed on a bench top tester from UTI.

Underfill Selection

Perhaps the most critical item governing flip-chip package reliability is the underfill, since it helps in the adhesion of the die to the substrate, and also provides reinforcement to the flipchip attach. There was added concern for this qualification due to the delicate nature of the Low-K dielectric on the die verses previous qualifications using FSG dielectric. So quite a bit of upfront work had to be done to select the appropriate underfill materials for this evaluation so at least one underfill would pass the 1st level and 2nd level reliability tests and the eventual qualification. The underfills were selected by looking at properties to address the Low-k dielectric issues (unlike the underfills used to qualify FSG die using high lead bumps) – Low Tg (~ 70 C), reduced modulus of elasticity (~ 8 GPa) and minimized CTE (~ 30 ppm/C). There was also concern about manufacturability issues (fast flow, void free, acceptable shelf and pot life), and dealing with 3 different sets of substrates – Alumina ceramic, HITCE ceramic and SLC laminate, which have different physical and adhesion properties.

Based on all of this, the following underfills were selected for 1st COL, 2nd COL and the qualification builds:

Table 1. Underfill properties.

Properties	Underfills								
	A	B	C	D	E	F	G	H	I
Modulus (GPa)	8.5	7.5	9.5	8.1	3.3	7.4	9	9.5	8
T_g (°C)	70	70	120	100	150	72	137	120	80
CTE < T_g (ppm/°C)	32	32	22	32	60	33	32	22	32
CTE > T_g (ppm/°C)	11	125	84	120	160	118	120	85	116
Filler Content (%)	55	58	64	58	20	55	55	65	60

Flux Selection

This is another critical item for flip-chip assembly. A variety of clean and no clean fluxes are used in the industry and so for the SLC laminate builds, a decision was made to try out both of these versions. The advantage of the no-clean flux is that process flow is simplified (since the parts do not have to go through a cleaner) and reduced thru-put. For the ceramic builds, cleaning was added to enable the use of a more active flux to improve wetting.

Assembly process

A special wafer saw process was developed for dicing low-K wafers to ensure that chip-outs, cracks and damage to the low-K layers are minimized. The rest of the process is fairly standard and basically unchanged from before.

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Bump geometry optimization experiment

As was discussed before, prior to any work with the underfill or other assembly related parameters, a screening experiment on non-underfilled parts was performed to understand and optimize the bump geometry for the die. This was done by creating a mask set with the different bump geometries in the four different quadrants, where the passivation opening, the top metal pad size and the Aluminum cap sizes, for a total of six different bump geometries are described in Table 2.

Table 2. Solder bump geometries.

Bump Type	Metal Pad	Passiva-tion Via	Alumi-num Cap	Under Bump Metallurgy
A	80 µm	76 µm	125 µm	110 µm
B	104 µm	90 µm	125 µm	110 µm
C	80 µm	55 µm	125 µm	110 µm
D	80 µm	40 µm	125 µm	110 µm
E	80 µm	76 µm	80 µm	110 µm
F	104 µm	90 µm	104 µm	110 µm

For this study, SLC laminate, HITCE ceramic and the Alumina ceramic substrates were used and included both the high lead and eutectic bumps, as follows:

Table 3. Solder bump geometry optimization experiment.

Leg No.	Bump Type		Substrate
	Eutectic	High Lead	
1	x		SLC
2		x	SLC
3	x		Alumna Ceramic
4		x	Alumna Ceramic
5	x		HITCE Ceramic
6		x	HITCE Ceramic

Ten parts from each leg were assembled without underfill and were subjected to Temperature Cycle (JEDEC condition B, -55 ^{o}C to 125 ^{o}C), with read points at approximately every 10 cycles until they failed electrically. These results are summarized in Tables 4 through 7. The SLC tests are not listed here since the results were not repeatable and conclusions couldn't be drawn from them. The value in the table represents the number of failing chains.

In addition to determining the optimum bump geometry based on the thermal cycling – condition B (T/C-B) data, the data indicated that the eutectic bumps are less sensitive to bump structure than high Pb bumps.

Table 4. Alumina ceramic data summary (High Pb).

Bump Type	Number of Failing Chains for All Packages				
	20	40	60	80	100
A					1
B					1
C			1	3	6
D				4	6
E	6	7	4	9	2
F		2	6	9	4

Table 5. Alumina ceramic data summary (Eutectic).

Bump Type	Number of Failing Chains for All Packages				
	20	40	60	80	100
A					2
B					1
C					2
D					
E				1	0
F			1	1	2

Table 6. HITCE ceramic data summary (High Pb).

Bump Type	Number of Failing Chains for All Packages	
	20 cycles	40 cycles
A	33	111
B	1	14
C	7	40
D	5	88
E	123	30
F	9	6

Table 7. HICE ceramic data summary (Eutectic).

Bump Type	Number of Failing Chains for All Packages	
	20 cycles	40 cycles
A		56
B		29
C		25
D		23
E		33
F	2	25

The results from the Alumna High Pb indicate that Legs A and B looked the best, with the chains failing after 100 T/C. For the HITCE legs, no trends and signals were seen with any of the bump geometries. So data from the Alumna legs was used to finalize the bump geometries. Between these two legs, design issues prevented the use of bump type B, so bump type A was chosen for the rest of the work.

Screening experiment or the 1st COL

The screening experiment was performed on all the three substrate types (Alumina ceramic, HITCE ceramic and the SLC laminate), and the DOE's were summarized in Tables 8 and 9.

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Table 8. Alumina ceramic and HITCE ceramic DOE.

Leg No.	Underfills							Bump Type	Number of Parts	
	A	B	C	D	E	F	G		TC-B*	HTS**
1	x							High Pb	11	11
2	x							Eutectic	11	11
3		x						High Pb	11	11
4		x						Eutectic	11	11
5			x					High Pb	11	11
6			x					Eutectic	11	11
7				x				High Pb	11	11
8				x				Eutetic	11	11
9					x			High Pb	11	11
10					x			Eutectic	11	11
11						x		High Pb	11	11
12						x		Eutectic	11	11
13							x	High Pb	11	11
14							x	Eutectic	11	11

* Temperature Cycle Condition. B
** High Temperature Storage 150 °C

Table 9. SLC laminate DOE.

Leg No.	Substrate		Underfills				Flux	SOP/ENIG	Bump Type	Number of Parts	
	SLC	New SLC	A	B	C	D				TC-B*	HTS**
1		x	x				A	Cu-SOP	High-Pb	77	45
2	x		x				A	Cu-SOP	Eutectic	22	22
3	x		x				A	ENIG	High-Pb	22	22
4	x		x				A	Cu-SOP	High-Pb	77	45
5	x			x			A	Cu-SOP	Eutectic	22	-
6	x			x			A	Cu-SOP	High-Pb	22	-
7	x				x		A	Cu-SOP	Eutectic	22	-
8	x				x		A	Cu-SOP	High-Pb	22	-
9	x					x	A	Cu-SOP	High-Pb	22	
10	x		x				B	ENIG	Eutectic	77	45
11		x	x				A	Cu-SOP	Eutectic	22	-
12		x	x				B	Cu-SOP	Eutectic	77	45
13	x		x				A	ENIG	High-Pb	77	45

Biased HAST on Legs 1,4,10,12 and 13 (15 parts per leg)
* Temperature Cycle Condition. B
** High Temperature Storage 150 °C

For this screening experiment, the T/C-B parts were subjected to preconditioning (level 3 for the ceramic substrates and level 4 for the SLC laminate), followed by temperature cycling of -55 °C to + 125 °C., with read points taken at 500, 1000, 1500 and 2000 cycles. The HTS parts had read points at 500, 1000, 1500 and 2000 hours.

The goal of the experiment is to select the best bump geometry, bump metallurgy, substrate material (old vs new for SLC) and material set technologies with the best chance for success for inclusion in the 2nd COL.

After reviewing the data and the CSAM results, a few strategic decisions had to be made. The first one being to evaluate only electrical test data from the optimum bump geometry (that the initial set of bump masks had six different geometries to see its effect on the reliability). The second was to review the reliability and CSAM results to determine the best and most robust legs. And finally, the materials sets had to be chosen based on their manufacturability and reliability. This had to be done for the 2nd COL since materials and the processes should be as close to the target process as possible in order to go with a high degree of confidence into the qualification knowing that this would just be a formality. The results of this experiment are summarized below:

Alumina Ceramic Results

T/C-B

Legs 1, 3 and 7 were stopped after 750 cycles due to poor electrical test results (in the area of the optimized bump geometry). Legs 9 and 11 were stopped at 1000 T/C for the same reason as above. Legs 5, 6, 13 and 14 were cycled to 2000 cycles and still passed electrical test and had good

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CSAM's as well. All the other legs (not mentioned here) were stopped due to either poor electrical test yields, manufacturing issues or poor yield after preconditioning. In conclusions, the best legs are:

- Leg 5 – High Pb bumps, Underfill C (Tg= 120C)
- Leg 6 – Eutectic bumps, Underfill C
- Leg 13 – High Pb bumps, Underfill G (Tg = 137C)
- Leg 14 – Eutectic bumps, Underfill G

High Temperature Storage

All of the legs continued on to 2000 hours of high temperature storage and there were no failures. All the CSAMs after 2000 hours also looked good. No signal is seen from this test.

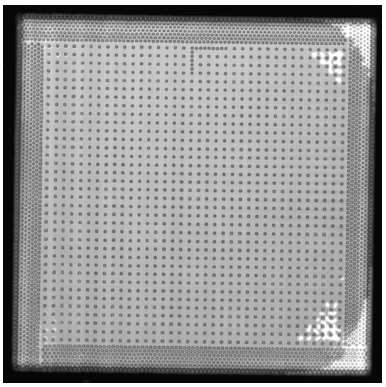

Figure 4. HITCE CSAM after 1000 T/C showing corner delamination.

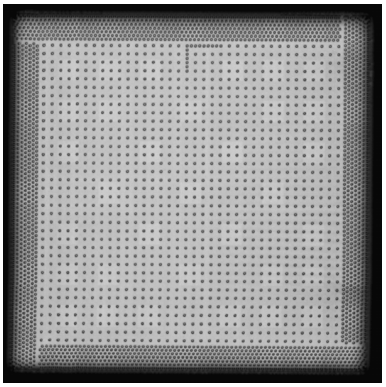

Figure 5. Good HITCE CSAM after 1000 T/C.

HITCE Ceramic Results

T/C-B

Legs, 1, 3, 9 and 14 were stopped after 500 cycles due to poor electrical test results. Legs 4, 11 and 13 were stopped after 1000 cycles. Legs 2, 5 and 6 looked good even after 2000 cycles and had good CSAM's as well. All the other legs were stopped either due to either poor electrical test yields, manufacturing issues or poor yield after preconditioning. Figures 4 and 5 illustrate examples of bad and good CSAM's send. In conclusions, the best legs are:

- Leg 2 – Eutectic bump, Underfill A (Tg = 70C)
- Leg 5– High Pb bumps, Underfill C (Tg = 120C)
- Leg 6 – Eutectic bumps, Underfill C

Figure 6 shows a good solder joint (after 1000 T/C).

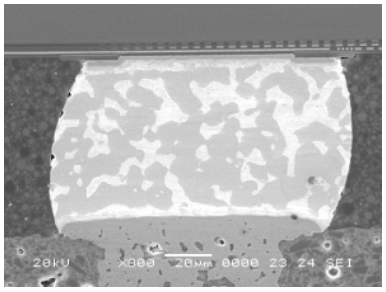

Figure 6. Example of a good solder joint after 1000 T/C.

High Temperature Storage

All of the legs continued on to 2000 hours of high temperature storage with no failures after electrical test. Also, all the CSAMs after 2000 hours looked good. No signal is seen from this test.

SLC Laminate Results

T/C-B

Legs 4, 5, 6, 7, 8, 9 and 13 were stopped after 1500 T/C due to numerous electrical failures. The rest of the legs were continued on to 2000 cycles. There were intermediate electrical test read points at 500 and 1000 cycles as well. Also, in the SLC (old material set), failures were observed in the stacked via on PTH and via on PTH structures. Legs 2, 3 and 11 were the best with all parts passing electrical test as well as having good CSAM results. Additionally, both the fluxes (clean and non-clean) looked good, and the Cu-SOP surface finish proved to be robust as well. Figure 6 shows a good solder joint and Figure 7 illustrates a failed solder joint. Examples of bad and good CSAM are illustrated in Figures 8 and 9.

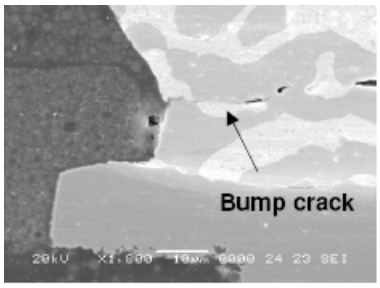

Figure 7. Bump crack after 1000 T/C – SLC.

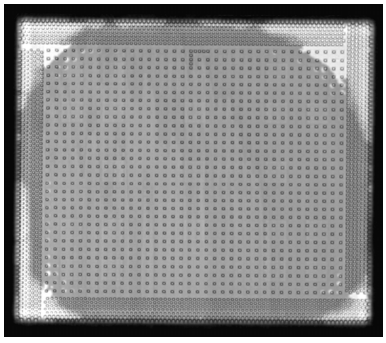

Figure 8. SLC CSAM after 1000 T/C showing corner delamination.

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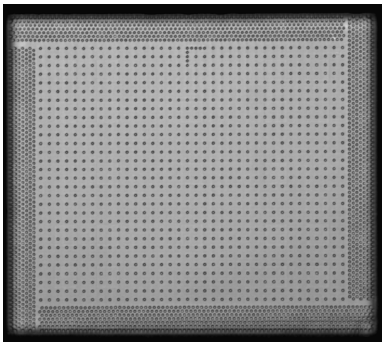

Figure 9. Good SLC CSAM 1000 T/C.

High Temperature Storage

All of the legs continued on to 2000 hours of high temperature storage with no failures. All the CSAMs after 2000 hours also looked good. No signal is seen from this test.

Biased HAST

There were no issues here since all the parts passed this test. CSAM's looked good as well.

In conclusion, the best legs for SLC were:

Leg 2 – Eutectic bumps, CuSOP, underfill A, SLC

Leg 3 – High Pb bumps, ENIG, underfill A, SLC

Leg 11– Eutectic bumps, CuSOP, underfill A, New SLC

Conclusions from 1st COL

Based on the results obtained from the 1st COL experiments, conclusions could be drawn on the process and materials that were needed to qualify the 90 nm Low K process, as listed below:

The High Pb and eutectic bumps looked good for all the substrate types.

For the SLC, the CuSOP with the new material set had good results.

Underfill A had good results with HITCE and SLC.

Assembly optimization or 2nd COL

The purpose of doing this evaluation was two-fold. First, the bump mask needed to be turned so that the optimized bump geometry could be used across the entire die. Second, the sample sizes were increased on the targeted processes to confirm the results from the 1st COL. For this set of experiments, the focus was narrowed to just the HITCE ceramic and the SLC laminate substrates. Due to the issue of electromigration and bump current carrying capacity associated with eutectic bumps, both the high-Pb and eutectic bumps were considered, even though the data from the 1st COL showed that the eutectic bumps were a lot more robust than the high-Pb bumps

For the SLC laminate substrates (which had many more variables in the 1st COL), the focus was further narrowed to using the SLC (new) laminate with Cu-SOP (no ENIG). Another advantage of using the new material set was that it is also ROHS compliant.

Based on all this, the bump masks were turned to get a new set of wafers with the optimized bump geometry – Bump Type A, the following DOE was derived:

Table 10. HITCE 2nd COL.

Leg No.	Underfill	Bump Type	Flux	Flux Clean	No. of Parts T/C-B
1	C	High Lead	A	Yes	40
2	C	High Lead	A	Yes	10
3	H	High Lead	A	Yes	68
4	D	High Lead	A	Yes	69
5	A	Eutectic	B	No	43

Please refer to Table 1 for the underfill properties. For the HITCE legs, Leg 3 used underfill H – which essentially has the same properties as underfill C, except that the viscosity is less and the flow is faster (to address manufacturing thru-put-time. Also for one of the legs (Leg 5), the flux was changed to a no-clean flux to see if cleaning after chip attach could be eliminated. Since the 1st COL reliability data for HTS was clean (no failures), the only test considered is preconditioning followed by T/C-B – again going up to 2000 cycles with intermediate read points at 1000, 1500 and 2000 cycles.

Table 11. SLC 2nd COL.

Leg No.	Underfill	Bump Type	Flux	Flux Clean	No. of Parts	
					T/C-B	Biased HAST
1	A	Eutectic	A	No	45	
2	A	Eutectic	B	Yes	45	22
3	I	Eutectic	B	Yes	45	22
4	A	High Pb	B	Yes	45	
5	D	High Pb	B	Yes	45	22
6	I	High Pb	B	Yes	45	22

For the SLC legs, a new underfill was added (underfill I), having recently been reformulated. As far as the fluxes go, two types of fluxes were looked at – clean and no-clean. Since the HTS data from the 1st COL was clean, only T/C-B and biased HAST were performed.

2nd COL Results

HITCE Ceramic

Here again the parts were subjected to JEDEC level 3 preconditioning, prior to temperature cycling. All the legs, except for Leg 4 performed very well (Leg 4 was stopped after 1000 cycles due to quite a few electrical failures). Leg 2 started having failures at 1500 cycles and Leg 1 had one part with increased resistance at 2000 cycles. Legs 3 and 5 had no failures even at 2000 cycles. Leg 5 was the best since the CSAM showed no delamination at all (Leg 3 showed slight corner delamination).

Based on these results, firm conclusions could be drawn for what the final material set and process parameters would be for the qualification build. So for the qualification, underfill A was chosen along with a non clean flux and eutectic bumps. The reason for going with the eutectic bumps is that our internal electromigration studies indicate that these would work with the designs[7].

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SLC Laminate

The parts were subjected to JEDEC Level 4 preconditioning, followed by T/C-B and biased HAST (as described in the Table 8). After 500 cycles, Leg #3 was stopped (since most of the parts failed electrical test). After 1000 cycles, Legs 5 and 6 were stopped – again due to electrical failures. Legs 1, 2 and 4 were continued on to 1500 and 2000 cycles. Legs 1 and 2 had one failure after 1500 cycles and 3 more after 2000 cycles. Leg 4 had no failures at 1500 cycles and 2 failures at 2000 T/C. CSAM showed some delamination around bumps. All the biased HAST legs passed.

Based on these results, firm conclusions could be drawn for the material set and process parameters for the qualification build. So for the qualification, the SLC (new material set) was chosen, along with Cu-SOP, underfill A, use of a no-clean flux and eutectic bumps.

Qualification

Since such a thorough job was done in performing all the preliminary work, running the JEDEC Q&R testing turned out to be just a formality to confirm our previous findings. Also, the results from the 2nd COL were so good, that there was really no reason to perform a verification build (which was planned at the start of this study). A decision was made to execute the qualification and run the full sample sizes with the frozen process and material sets for HITCE ceramic and SLC Laminate as listed in Table 12.

Table 12. Final substrate and process specifications.

	HITCE Ceramic	SLC Laminate
Surface Finish	Electroless Ni and Au	Cu-SOP
Bump Type	Eutectic	Eutectic
Underfill	A	A
Flux Type	No Clean	No Clean

Even though Underfills C and H performed very well (with the high lead bumps) for the HITCE packages, manufacturing issues precluded their use (viscosity was significantly higher than the other underfills resulting in slower throughput at the underfill operation and the possibility of void inclusions). So the eutectic bumps with the underfill A was chosen for this process. The qualification results are listed in Table 13 for both HITCE and SLC.

Table 13. Qualification results.

Reliability Tests	HITCE Ceramic	SLC Laminate
Popcorning	0/10	0/10
Temperature Cycle Condition B, 1000 cycles	0/77	0/77
High Temperature Storage, 1000 hrs, 150 °C	0/45	0/45
Biased HAST 96 hours, 130 °C, 85% RH, 3.3 V	0/45	0/45

#Fail / Total # part

All of these parts were assembled using the standard production flow. The assembly yields for both of these substrate types were in the 99%+ range, with excellent process controls. The underfill coverage was excellent, CSAM examples of some them are included here (Figures 10, 11 and 12).

The temperature cycling test was continued until 1500 cycles for both the substrate types with again no electrical fails, demonstrating the robustness of the process and materials set selected for the qualification.

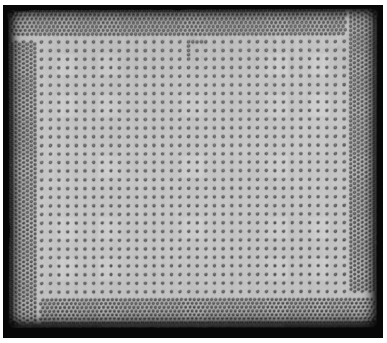

Figure 10. SLC CSAM after 1000 T/C.

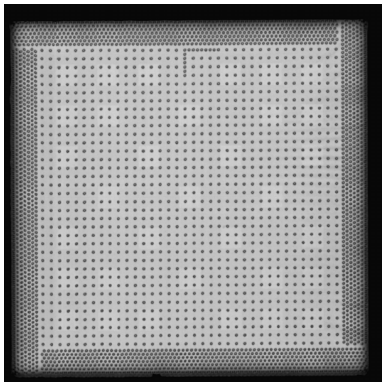

Figure 11. HITCE CSAM after Biased HAST.

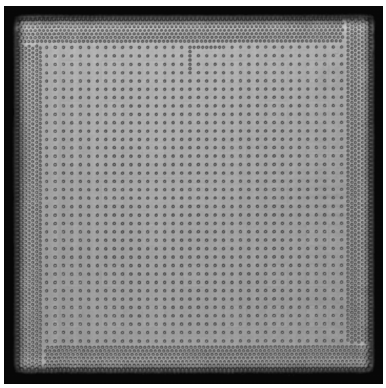

Figure 12. HITCE CSAM after 1000 T/C.

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Conclusions

It has been shown that by using a systematic approach, Avago Technologies can tackle a challenging project using Low-K silicon and qualify it successfully. The data also indicates that eutectic bumps are more robust than high lead bumps, and if current carrying capacity had dictated the product need, high lead bumps could have been used for the qualification builds. The process robustness was demonstrated by extending the reliability tests beyond what is required by JEDEC and a common underfill was utilized for both the HITCE ceramic and the SLC laminate substrates with a no-clean flux.

As a next step, a similar approach is planned when addressing the next qualification projects (lead reduced flip-chip, thin core and 65 nm flip-chip).

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